

New Challenge - DDR2 Module Testing

By: Cecil Ho CST, Inc. October 2004



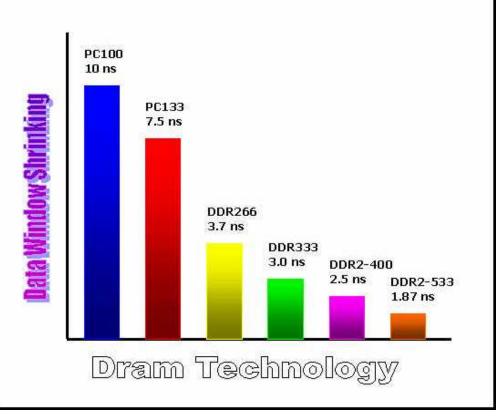
DDR2 Module Difference

- Vcc = SSTL 1.8V Vs SSTL 2.5V
- BGA package Vs TSOP
- Post Cas to fill pipeline efficiently
- Differential DQS Vs Single Ended
- ODT On Die Termination
- OCD Off Chip Driver Control



Higher Frequency, Less Margin, & Cycle Time

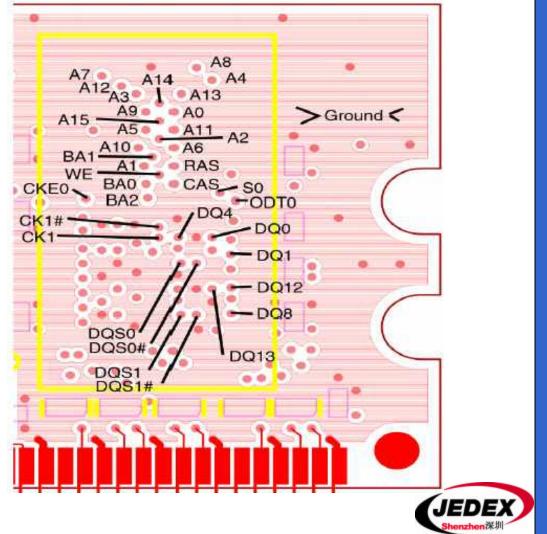
- Data window shrinking
- PC100 = 10ns
- PC133 = 7.5ns
- DDR 266 = 3.7ns
- DDR 333 = 3.0ns
- DDR2 400 = 2.5ns
- DDR2 533 = 1.87ns





BGA Package Creates Probing Problem

Probe points are hard to get to.



BGA Package are Creating Mechanical Problem

 Mechanical balls were added to give strength.
 But is it enough?

| A 00 | 4 5 6 7 8 9 |
|--------------|--------------------|
| 18 | 1999-1997 C. C. C. |
| c | 2-11 0008/07/27 |
| D 000 | 000 |
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| AA 🔘 🔘 | O OT |
| АВ 🔘 🥵 | O G |



Motherboard Test No Longer Effective

- Open/Short circuit cause no POST, test cannot continue
- Short circuits might damage mother board
- Test result vary from board to board
- Hide some problem if not careful



Open/short Major Issue, Low Cost Tester to Help

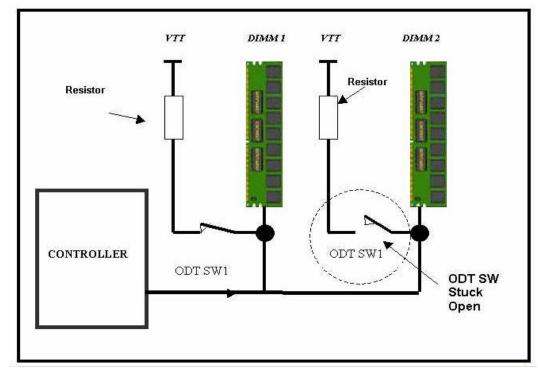
- Walk address test pattern to detect address problem
- Walk data test to pinpoint data line problem
- Marching test to cycle out bad cells and cross talk error
- Control line tests to ensure control line integrity.





ODT Problem Not Detected on Motherboard

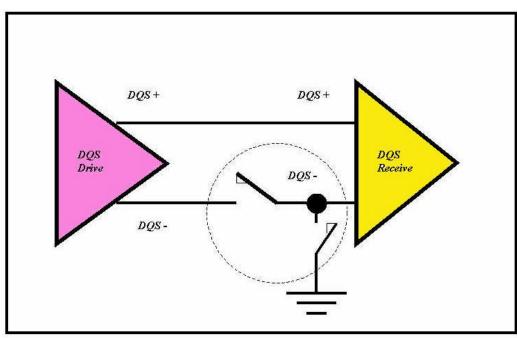
 Cross Vtt bias from another module might allow module to function even when ODT switch is opened.





Differential DQS Fault Not Detected

- One side of the differential DQS can be shorted to ground, module still work
- One side of differential DQS can be open, module still work.





DDR2 DIMM Test Focus -Detecting Broken Joints

- Functional test a must detecting address and data failure
- Control line test a must detecting CS, DM, WE, Ras, Cas line problems
- Special algorithm for testing ODT, OCD and DQS lines



The SPD Challenge

- DDR2 SPD requires SWP
- New chips has RSWP

| | PIN | | | Preamble | | | | | | RW | |
|------------|-----|----------|-----|----------|----|----------|----|-----|-----|-----|----|
| Command | A2 | A1 | A0 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| SET PSWP | SA2 | SA1 | SA0 | 0 | 1 | 1 | 0 | SA2 | SA1 | SA0 | 0 |
| SET RSWP | 0 | 0 | VHV | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| CLEAR RSWP | 0 | 1 | VHV | 0 | 1 | | 0 | 0 | 1 | 1 | 0 |

| | Min | Max | Units | | |
|-----|-----|-----|-------|-----------------------|--|
| VHV | 7 | 10 | V | Note: VHV-VCC > 4.8 V | |



Fault Focusing

- Since BGA does not allow visual inspection of joints
- Special algorithm added to pin point problem and location

| Show Data | 30 TestNo: 3 25 Reset | | * |
|------------------------------------|--|---|---|
| Module | : DDR2 32M×64 256MB1B(4)@2×266MHZ 1.8V | | |
| Addr.(rowxcol.) Data (bankxbit) | :13×10 :1×64 | | |
| Internal Banks | : 1×04 | | |
| | : Mode=Sequential, Burst length=4 | | |
| | : CL=4, AL=0, Trcd=4, Trp=4 | | |
| Test Loop # | :1 | | |
| ## FAIL: wk_data - | Loop 1 ## | | |
| Bank 1 : 0, 24-3 | 1. | 5 | |
| Daux : - 0, 24-3 | : 00:00:00.904 | | |



Gentle Test Handling Required

- Automatic handler eliminates
 human error
- It utilize soft landing and output stacker.
- Automatic handler greatly reduce breakage







