IDT

Powering What's Next

Register Validation Board

A test board for verifying register timing on DDRII DIMM modules

This board can also be used for basic DIMM addressing tests

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Sponsored by the JC40
Test and Validation Task Group

Stan Hronik

Register Test and Validation Board

- **Register T&V board's DIMM socket accepts**
  - **Special test cards w/probe points for register testing**
  - **Registered DIMMs**
  - **Stacked DIMMs**
  - **Un-buffered DIMMs**
- **Register T&V Board will provide regardless of DIMM type**
  - **Address patterns**
  - **Control patterns**
  - **Clock signal**

All signals at the DIMM connector are tuned to be clean and simulate a motherboard environment.

T&V board may be used as a DIMM debug tool

Modes of Operation

1. “Realistic” DIMM Operation
   - DIMM initialization
     - Automatic on power up
     - Repeated whenever requested
   - Legitimate address and control for both reads and writes
     - Many address test patterns available
     - Must be programmed into the EPROM
   - DIMM reset recovery
   - Signal positioning tests relative to clock
     - Limits of address signal placement
     - Limits of control signal placement
   - Register “banging” tests with real SDRAM cycles
2. “Banging” Register Test Patterns
   - “Banging” tests for extreme register situations
     - Examples are: SSO, & Ground bounce
   - DIMM sequencing and control is ignored

Test Variable Controls

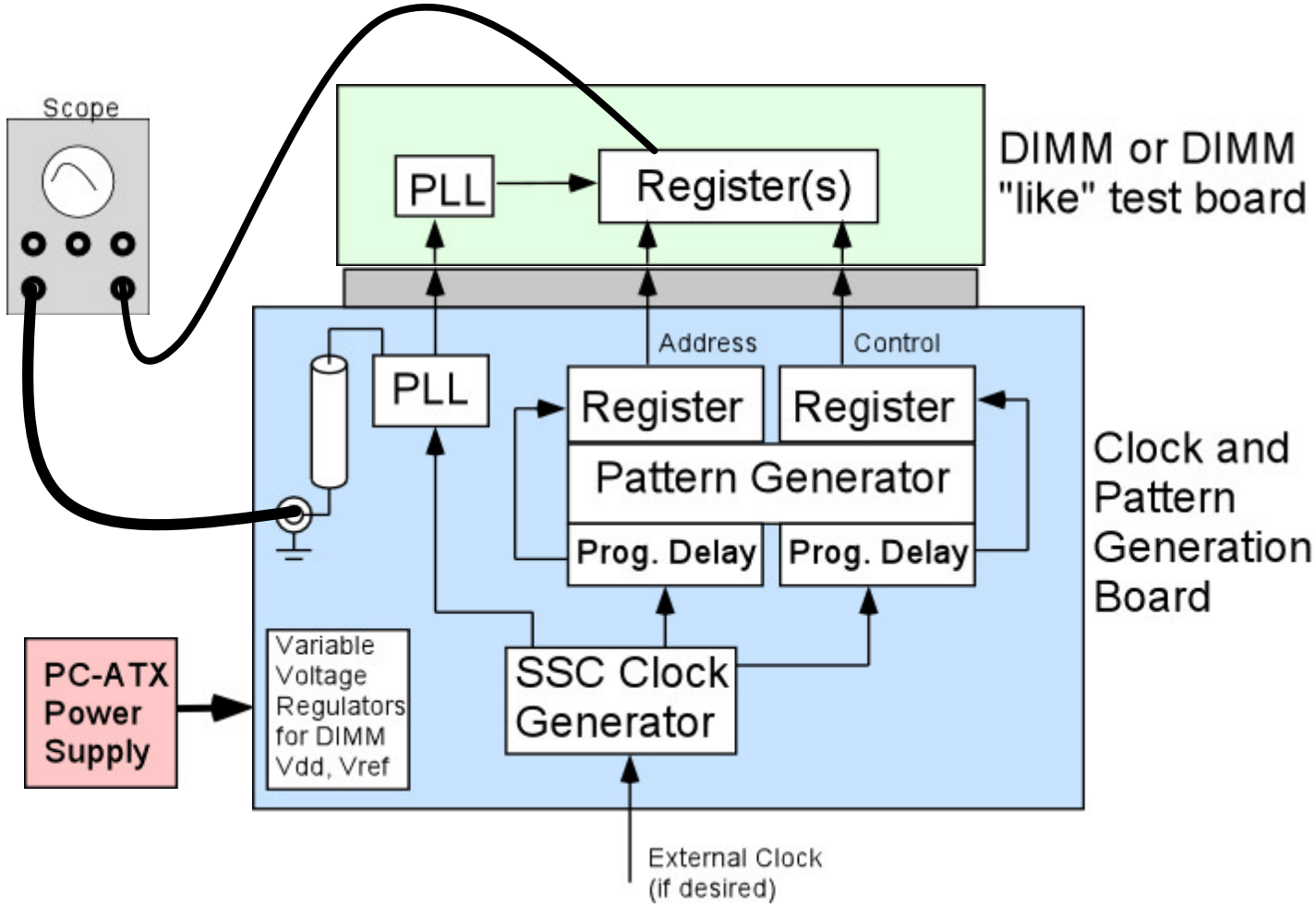
- **Test Pattern Selection**
  - **Capable of selecting up to 256 different patterns**
- **DIMM Operation at Corner Voltages**
  - **Vdd adjustable/restricted to DIMM limits**
  - **Vref adjustable to DIMM limits**
  - **Motherboard voltages not affected, to maintain integrity of tests**
- **Operation at multiple Clock Frequencies**
  - **Selection of Internal or External clock**
  - **Spread Spectrum On/Off**
- **Skewing**
  - **Address relative to clock**
  - **DIMM control relative to clock**
- **Board reset**
  - **Reset during power up**
  - **Push button reset (loads new patterns)**

Selected Register Parameters Evaluation

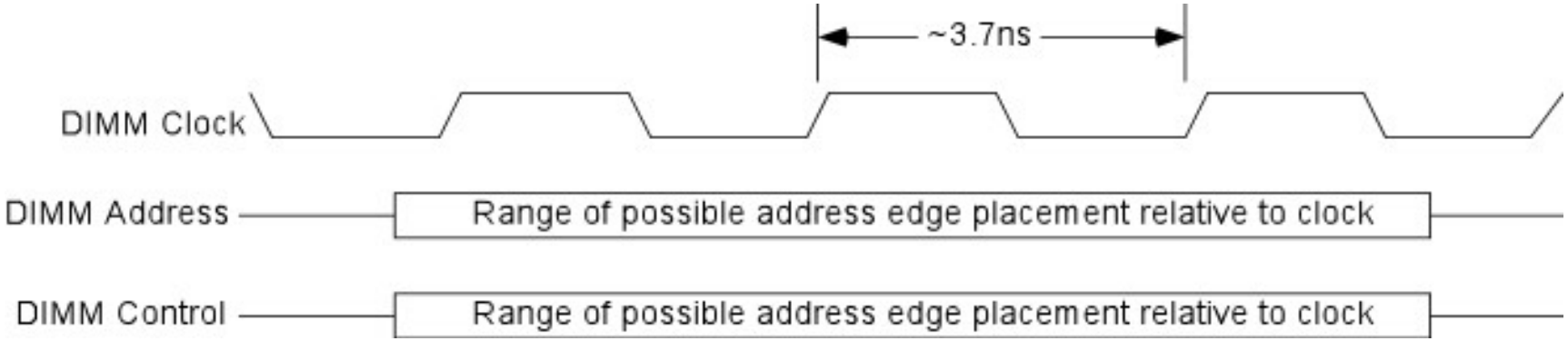
- Register Propagation Delays
- Register Setup and Hold Times
  - CKE, ODT, Reset and CS
  - Address
  - 10ps increments (1024 total steps)
- Effects of skewing CKE, ODT and CS relative to address and clock
- Simultaneous Switching Delay, Ground/Vdd Bounce
- Signal integrity at virtually any point
  - Register Output/ DRAM Input
  - Register Clock Input
  - Data lines don't toggle

T&V Board provides the chassis for your DIMM & Register test

Block Diagram and Test Configuration



Programmable Positioning of Address and Control Signals



- **Signals are broken into three independent skew groups**
  - **DIMM clock (zero reference point, no skew)**
  - **Address – A, BA, WE#, RAS#, CAS#**
  - **Control -- Reset#, S1#, CKE1, ODT1, S0#, CKE0, ODT0**
- **Skew is set through two banks of 10 bit DIP Switches**
  - **10ps increments to signal positioning**
  - **1024 steps possible**
  - **10ns total skew range**
    - **For all frequencies above 100MHz, skew can be set over more than a full clock cycle**
    - **At 266 MHz, the skew can be over almost three cycles**

Test Patterns

(Supported in both "Realistic" and "Banging" modes)

- **Initialization Patterns**
  - **DIMM Initialization**
  - **Synchronization**
    - **One bit high every fourth cycle**
- **"Walking Patterns**
  - **Walking "1", SDRAM Read**
  - **Walking "0", SDRAM Read**
  - **Walking "1", SDRAM Write**
  - **Walking "0", SDRAM Write**
- **Setup and Hold Patterns**
  - **CKE, CS, ODT etc**
    - **relative to clock**
    - **relative to address**
  - **Address relative to clock**

256 Different Patterns Possible

- **Test Patterns for Noise (both Read and Write)**
  - **All bits switching**
  - **No bits switching**
  - **All bits switching, one inverted**
  - **Ground Bounce**
    - **All bits switching except one held low**
  - **Vdd Bounce**
    - **All bits switching except one held high**
  - **ISI**
    - **Number of bits switching increases each cycle**
  - **Simultaneous Switch Delay**
    - **One bit vs all bits switching**
- **Any Other Suggested Pattern**

All patterns are 512 vectors, then repeat (except initialization)

Board Operation

- Make physical connections
  - Power, probes, DIMM
- Select clocking schemes
  - 200MHz, 266MHz or External clock
  - SS on, SS off (internal clock only)
- Apply Power
  - Board will power up and initialize DIMM
  - DIMM and testing functional at this point
- Adjust DIMM voltages as desired
  - Vdd, Vref
- Set Skews relative to clock as desired
  - Address register, Control register
- Select test patterns as desired
  - Push reset to load new pattern
  - May reinitialize DIMM if desired
- Enjoy the picture in your oscilloscope
  - Start “tweaking” parameters

Pin Skew Control

FIFO	FIFO INPUT SIGNAL	Register	DDR II DIMM Pin
CONTROL	CFIFO_DIN[6]	CONTROL	RESET#
	CFIFO_DIN[5]		S1#
	CFIFO_DIN[4]		CKE1
	CFIFO_DIN[3]		ODT1
	CFIFO_DIN[2]		S0#
	CFIFO_DIN[1]		CKE0
	CFIFO_DIN[0]		ODT0
DATA	DFIFO_DIN[21]	DATA	A15
	DFIFO_DIN[20]		A14
	DFIFO_DIN[19]		A13
	DFIFO_DIN[18]		A12
	DFIFO_DIN[17]		A11
	DFIFO_DIN[16]		A10
	DFIFO_DIN[15]		A9
	DFIFO_DIN[14]		A8
	DFIFO_DIN[13]		A7
	DFIFO_DIN[12]		A6
	DFIFO_DIN[11]		A5
	DFIFO_DIN[10]		A4
	DFIFO_DIN[9]		A3
	DFIFO_DIN[8]		A2
	DFIFO_DIN[7]		A1
	DFIFO_DIN[6]		A0
	DFIFO_DIN[5]		BA2
	DFIFO_DIN[4]		BA1
	DFIFO_DIN[3]		BA0
	DFIFO_DIN[2]		WE#
	DFIFO_DIN[1]		RAS#
	DFIFO_DIN[0]		CAS#

Clocking Configurations

- On board clock generator provides two DIMM clock frequencies
  - 266MHz (DDR533)
  - 200MHz (DDR400)
  - Others available but not guaranteed (DIMM limits testing)
- Spread Spectrum 33kHz down spread available
  - Can be turned on or off when using internal clock
  - Triangular modulation
- Available external clock connection point which allows
  - Any DIMM clock frequency from 100 to 270 MHz
    - External applied clock is half the DIMM frequency (50 – 135MHz)
    - If the clock is external the SSC must also be external
  - "Experimenting" with lower frequencies if needed for DIMM debug
- Clock reference point
  - Attachment point for clock test/sync probe
  - Probe has no effect on DIMM PLL or signal integrity
  - Unnecessary to develop test points on DIMM for clock
  - Phase aligned with clock at register input

Additional Required Test Equipment

- **Standard PC-ATX power supply**
  - **Minimum power output is sufficient**
- **High speed oscilloscope**
  - **4G sampling or better recommended**

Contact Information

- **Test Patterns and Board Technical Information**
  - **Stan Hronik, hronik@idt.com, (408) 654-6776**
  - **John Smolka, jsmolka@idt.com, (408) 654-6539**
- **Board Availability**
  - **Oliver Kiehl, oliver.kiehl@infineon.com, (802) 764-1959**
- **DDR2 and TV Board Component Support**
  - **Sergis Mushell, sergis.mushell@idt.com, (408) 654-8423**

Summary

- **The Register T & V board provides a highly integrated testing environment.**
  - **A minimum of test equipment is required**
  - **Many onboard test stimuli are available**
    - **Patterns**
    - **Skew**
    - **Voltage**
    - **Frequency**
  - **The user provides the test (on the DIMM)**
    - **Possible tests are unlimited**