SPD Comparison PC100/PC133: 16Mx72 Registered DIMM

This SPD table is intended to represent all of the combinations which a system BIOS programmer may expect when using both PC133 and PC100 16Mx72 Registered DIMMs. This is intended to be an example only, there are other combinations which may be utilized if the SDRAMs display different characteristics. (For example, a 256Mbit SDRAM has a different refresh rate which would change Byte 12)

The following speed sort combinations are included in this comparison:
--133MHz-333(CL, tRCD,tRP)
--133MHz-333 and 100MHz-322
--133MHz-333 and 100MHz-322/222
--100MHz-322
--100MHz-222

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Serial Presence Detect (Part 1 of 4)

Byte #	Description	Old PC133 (133MHz-333 only)		Finalized PC133 (133MHz-333, 100MHz-322)		PC133 Other (133MHz-333, 100MHz-322/222)		PC100 (100MHz-322)		PC100 (100MHz-222/322)		Notes
		SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	
0	Number of Serial PD Bytes Written during Production	128	80	128	80	128	80	128	80	128	80	
1	Total Number of Bytes in Serial PD device	256	08	256	08	256	08	256	08	256	08	
2	Fundamental Memory Type	SDRAM	04	SDRAM	04	SDRAM	04	SDRAM	04	SDRAM	04	
3	Number of Row Addresses on Assembly	12	0C	12	0C	12	0C	12	0C	12	0C	
4	Number of Column Addresses on Assembly	10	0A	10	0A	10	0A	10	0A	10	0A	
5	Number of DIMM Banks	1	01	1	01	1	01	1	01	1	01	
6 - 7	Data Width of Assembly	x72	4800	x72	4800	x72	4800	x72	4800	x72	4800	
8	Assembly Voltage Interface Level	LVTTL	01	LVTTL	01	LVTTL	01	LVTTL	01	LVTTL	01	
9	SDRAM Device Cycle Time (CL = 3)	7.5ns	75	7.5ns	75	7.5ns	75	10.0ns	A0	10.0ns	A0	1, 2
10	SDRAM Device Access Time from Clock at CL=3	5.4ns	54	5.4ns	54	5.4ns	54	6.0ns	60	6.0ns	60	
11	DIMM Configuration Type	ECC	02	ECC	02	ECC	02	ECC	02	ECC	02	
12	Assembly Refresh Rate/Type	SR/1X (15.625µ)	80	SR/1X (15.625µ)	80	SR/1X (15.625µ)	80	SR/1X (15.625µ)	80	SR/1X (15.625µ)	80	
13	SDRAM Device Width	x4	04	x4	04	x4	04	x4	04	x4	04	

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{\text{CAS}}$ latency).
2. Minimum application clock cycle time is 7.5ns (133MHz) or 10.0ns (100MHz).
3. cc = Checksum Data byte, 00-FF (Hex).
4. ww = Binary coded decimal week code, 01-51 (Decimal) ‘ 01-34 (Hex).
5. yy = Binary coded decimal year code, 0-00 (Decimal) ‘ 00-63 (Hex).
6. ss = Serial number data byte, 00-FF (Hex).
7. These values apply to PC100 applications only.

Serial Presence Detect (Part 2 of 4)

Byte #	Description	Old PC133 (133MHz-333 only)		Finalized PC133 (133MHz-333, 100MHz-322)		PC133 Other (133MHz-333, 100MHz-322/222)		PC100 (100MHz-322)		PC100 (100MHz-222/322)		Notes
		SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	
14	Error Checking SDRAM Device Width	x4	04	x4	04	x4	04	x4	04	x4	04	
15	SDRAM Device Attr: Min Clk Delay, Random Col Access	1 Clock	01	1 Clock	01	1 Clock	01	1 Clock	01	1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported	1, 2, 4, 8, Full Page	8F	1, 2, 4, 8, Full Page	8F	1, 2, 4, 8, Full Page	8F	1, 2, 4, 8, Full Page	8F	1, 2, 4, 8, Full Page	8F	
17	SDRAM Device Attributes: Number of Device Banks	4	04	4	04	4	04	4	04	4	04	
18	SDRAM Device Attributes: $\overline{CAS}$ Latencies	3	04	2, 3	06	2, 3	06	2, 3	06	2, 3	06	
19	SDRAM Device Attributes: $\overline{CS}$ Latency	0	01	0	01	0	01	0	01	0	01	
20	SDRAM Device Attributes: $\overline{WE}$ Latency	0	01	0	01	0	01	0	01	0	01	
21	SDRAM Module Attributes	Reg/Buf with PLL	IF	Reg/Buf with PLL	IF	Reg/Buf with PLL	IF	Reg/Buf with PLL	IF	Reg/Buf with PLL	IF	
22	SDRAM Device Attributes: General	Write-1/ Read Burst, Pre-charge All, Auto-Pre-charge	0E	Write-1/ Read Burst, Pre-charge All, Auto-Pre-charge	0E	Write-1/ Read Burst, Pre-charge All, Auto-Pre-charge	0E	Write-1/ Read Burst, Pre-charge All, Auto-Pre-charge	0E	Write-1/ Read Burst, Pre-charge All, Auto-Pre-charge	0E	
23	Minimum Clock Cycle at CLX-1 (CL = 2)	N/A	00	15.0ns	A0	10.0ns	A0	15.0ns	F0	10.0ns	A0	1, 2
24	Maximum Data Access Time (t_{AC}) from Clock at CLX-1 (CL = 2)	N/A	00	9.0ns	90	6.0ns	60	9.0ns	90	6.0ns	60	
25	Minimum Clock Cycle Time at CLX-2 (CL = 1)	N/A	00	N/A	00	N/A	00	N/A	00	N/A	00	

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2. Minimum application clock cycle time is 7.5ns (133MHz) or 10.0ns (100MHz).
3. cc = Checksum Data byte, 00-FF (Hex).
4. ww = Binary coded decimal week code, 01-51 (Decimal) ‘ 01-34 (Hex).
5. yy = Binary coded decimal year code, 0-00 (Decimal) ‘ 00-63 (Hex).
6. ss = Serial number data byte, 00-FF (Hex).
7. These values apply to PC100 applications only.

Serial Presence Detect (Part 3 of 4)

Byte #	Description	Old PC133 (133MHz-333 only)		Finalized PC133 (133MHz-333, 100MHz-322)		PC133 Other (133MHz-333, 100MHz-322/222)		PC100 (100MHz-322)		PC100 (100MHz-222/322)		Notes
		SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	
26	Maximum Data Access Time (t_{AC}) from Clock at CLX-2 (CL = 1)	N/A	00	N/A	00	N/A	00	N/A	00	N/A	00	
27	Minimum Row Pre-charge Time (t_{RP})	23ns (22.5ns)	17	20.0ns	14	20.0ns	14	20.0ns	14	20.0ns	14	
28	Minimum Row Active to Row Active delay (t_{RRD})	15.0ns	0F	15.0ns	0F	15.0ns	0F	20.0ns	14	20.0ns	14	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD})	23ns (22.5ns)	17	20.0ns	14	20.0ns	14	20.0ns	14	20.0ns	14	
30	Minimum $\overline{RAS}$ Pulse width (t_{RAS})	45.0ns	2D	45.0ns	2D	45.0ns	2D	50.0ns	32	50.0ns	32	
31	Module Bank Density	128MB	20	128MB	20	128MB	20	128MB	20	128MB	20	
32	Address and Command Setup Time Before Clock	1.5ns	15	1.5ns	15	1.5ns	15	2.0ns	20	2.0ns	20	
33	Address and Command Hold Time After Clock	0.8ns	08	0.8ns	08	0.8ns	08	1.0ns	10	1.0ns	10	
34	Data Input Setup Time Before Clock	1.5ns	15	1.5ns	15	1.5ns	15	2.0ns	20	2.0ns	20	
35	Data Input Hold Time After Clock	0.8ns	08	0.8ns	08	0.8ns	08	1.0ns	10	1.0ns	10	
36 - 61	Reserved	Un-defined	00	Un-defined	00	Un-defined	00	Un-defined	00	Un-defined	00	
62	SPD Revision	JEDEC 2	02	JEDEC 2	02	JEDEC 2	02	PC100 Rev1.2A	12	PC100 Rev1.2A	12	
63	Checksum for bytes 0 - 62		cc		cc		cc		cc		cc	3
64 - 71	Manufacturers' JEDEC ID Code											
72	Assembly Manufac-turing Location											
73 - 90	Assembly Part Number											
91 - 92	Assembly Revision Code											
93 - 94	Assembly Manufac-turing Date		yyww		yyww		yyww		yyww		yyww	4, 5

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Serial Presence Detect (Part 4 of 4)

Byte #	Description	Old PC133 (133MHz-333 only)		Finalized PC133 (133MHz-333, 100MHz-322)		PC133 Other (133MHz-333, 100MHz-322/222)		PC100 (100MHz-322)		PC100 (100MHz-222/322)		Notes
		SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	SPD Entry Value	SPD Entry HEX	
95 - 98	Assembly Serial Number		ss		ss		ss		ss		ss	6
99 - 125	Reserved	Un-defined	00	Un-defined	00	Un-defined	00	Un-defined	00	Un-defined	00	
126	Module Supports this Clock Frequency	Reserved	64	Reserved	64	Reserved	64	100MHz	64	100MHz	64	7
127	Attributes for clock frequency defined in Byte 126	Reserved	85	Reserved	85	Reserved	87	CLK0, CL=3, ConAP	85	CLK0, CL=2, 3, ConAP	87	7
128 - 255	Open for Customer Use	Unde-fined	00	Unde-fined	00	Unde-fined	00	Unde-fined	00	Unde-fined	00	

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7. These values apply to PC100 applications only.